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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P5727
First Inventor or Application Identifier	Nhon Toai Quach
Title	ERROR RECOVERY FOR SPECULATIVE MEMORY ACCESSES
Express Mail Label No.	EL466331030US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [Total Pages 14]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [Total Sheets 2]

4. Oath or Declaration [Total Pages 6]
   a. ☐ Newly executed (original copy)
   b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Copy
   b. ☐ Paper Copy (identical to computer copy)
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☒ Information Disclosure Statement (IDS)/PTO - 1449 ☒ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
14. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. ☐ Other: .....

16. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No:

Prior application Information. Examiner _____ *Group/Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
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Country	U.S.A.	Telephone	(714) 557-3800	Fax	(714) 557-3347

Name (Print/Type)	James Henry, Reg. No. 41,064		
Signature		Date	09/30/00

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See 37 C F R §§ 1 27 and 1 28

TOTAL AMOUNT OF PAYMENT ($) 768.00

Complete if Known	
Application Number	
Filing Date	September 30, 2000
First Named Inventor	Nhon Toai Quach
Examiner Name	
Group/Art Unit	
Attorney Docket No.	042390.P5727

JC841 U.S. PTO 09/676311 09/30/00

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees to
   ☒ The Commissioner is hereby authorized to credit any over payments to

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

☒ Charge Any Additional Fees Required Under 37 CFR §§ 1 16,1 17, 1 18 and 1 20

2. ☒ Payment Enclosed:
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	$690.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	20	- 20 =	0	X	18.00	=	0
Independent Claims	4	- 3 =	1	X	78.00	=	$78.00
Multiple Dependent						=	

***or number previously paid, if greater, For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple Dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 78.00

FEE CALCULATION (continued)

3. ADDITIONAL FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	*Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	*Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,210	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____
Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	James Henry			Reg. Number	41,064
Signature		Date	09/30/00	Deposit Account User ID	02-2666

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Atty Ref: 042390.P5727
Express Mail No. EL466331030US

UNITED STATES PATENT APPLICATION

FOR

ERROR RECOVERY FOR SPECULATIVE MEMORY ACCESSES

Inventors:

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Prepared by:

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ERROR RECOVERY FOR SPECULATIVE MEMORY ACCESSES

FIELD OF THE INVENTION

This invention relates to computer memory error recovery and, more particularly, to error recovery from errors detected during speculative memory accesses.

BACKGROUND OF THE INVENTION

A general purpose computer uses a central processor unit (CPU) to perform instructions on data. The instructions to be executed and the data required by those instructions are read from a computer memory. The overall speed of the computer is affected both by the speed at which the CPU can execute instructions and the speed at which the memory can provide instructions and data to the CPU. To improve the speed at which instructions and data are supplied by the memory, modem computers often issue and complete memory transactions speculatively. That is, the processor predicts what instructions and data are likely to be needed in the near future and the memory is accessed to obtain instructions and/or data prior to the actual requirement for the speculatively accessed memory contents.

Computer memories are subject to a variety of transient failures that result in corruption of the content of a particular memory location. While such transient corruption is infrequent, the consequences of such corruption, particularly if the content represents an instruction to be executed, can be catastrophic to the proper execution of a computer program. Computers may include means to detect errors in the contents retrieved by a memory access. There may be further means to correct at least some detected errors. Such error detecting and correcting means generally introduce a substantial delay in the processing when an error is detected. Uncorrected errors may require abnormal termination of an executing program. Simplicity and low-cost in error recovery processing is favored over speed because memory errors are encountered infrequently.

In a computer that uses speculative memory accesses, memory errors may be detected during a speculative memory access. A significant proportion

of the memory accesses may be speculative accesses in a computer that uses speculative accesses. A significant proportion of the speculative accesses may be for memory contents that will not be used by the CPU during the time the contents are available from the speculative access. The delays introduced by the error recovery processing for speculatively accessed corrupted memory contents adds an unnecessary overhead when the contents are not actually required by the CPU. An uncorrectable error detected during a speculative access can cause a potentially unnecessary abnormal termination of an executing program.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a computer system that embodies the invention.

Figure 2 is a flowchart of the method of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Memory includes any source of instructions and/or data that a machine, such as a computer, can access. Memory can include, but is not limited to, cache memory including both tags and data, random access memory (RAM), read-only memory (ROM), bulk storage devices such as fixed or removable disks including both read-write and read-only devices, and network devices that provide data accessed from other computers or other devices not directly part of the accessing computer.

A machine-readable medium includes any mechanism that provides, stores, or transmits information in a form readable by a machine, such as a computer. A machine-readable medium includes, but is not limited to, read only memory (ROM), random access memory (RAM), magnetic disk storage media, optical storage media, flash memory devices, and electrical, optical, acoustical or other form of propagated signals, such as carrier waves, infrared signals, or digital signals.

Logical indications such as true and false include any form of information that is defined and interpreted to indicate a particular logical condition. For example, a single bit flag has two logical states, commonly indicated as 0 and 1. The logical state 0 of such a flag may indicate false in one embodiment of a logical indication. In another embodiment, 0 may indicate true. Logical indications may have more than two states with particular values defined to indicate particular logical states.

A system is a combination of devices that includes a machine, and a memory coupled to the machine. A system may include additional elements in support of the machine and memory such as error detection mechanisms. A machine, such as a computer for example, that loads data values from a memory may use an error detecting mechanism for detecting errors in the values loaded from the memory. Errors are differences between the value as stored into the memory and the value as loaded from the memory. These errors may be "soft" errors that occur intermittently due to cosmic ray and alpha particle bombardment of the memory device. An example of a mechanism for detecting errors is a parity bit associated with a memory value. The error detecting mechanism may also provide for correcting some errors. An example

of such a mechanism is an error correcting code (ECC) associated with a memory value. The error detecting mechanism may provide a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory. A cache memory error on a line that is clean or shared can be corrected by invalidating the line. If the line is dirty, then the error is not recoverable.

Figure 1 shows a computer system that embodies the invention. The exemplary system may include a machine 10 coupled to a read-only memory 18, a random access memory 22, and one or more peripheral devices 24 by a bus 16. Instructions for an error handler 20 according to the present invention may be stored in the read-only memory 18 which when executed by the machine 10, cause the machine to perform operations to respond to memory error indications and provide recovery from the memory error. The memory error handler may be executed by the machine when a memory load request returns a value retrieved from the memory with the memory fault indication set true. If the memory error handler is unable to correct the memory error, recovery may be termination of the program that issued the memory load request. If the memory error handler is able to correct the memory error, recovery may require a lengthy sequence of instruction to perform the correction.

Figure 2 shows a flowchart of instruction execution for a memory error handler that embodies the present invention. The memory error handler receives a memory fault indication 100. If the memory fault indication is not true there is no memory error to be handled and the memory error handler returns 104 without performing any error handling. It will be appreciated that in other embodiments the memory error handler will not be executed unless there is a memory fault indication and the memory error handler may not receive or test the memory fault indication since that test will have occurred outside the memory error handler.

The memory error handler according to the present invention may handle errors generated by speculative loads differently from errors generated by non-speculative loads. If the memory load request is speculative, the memory value is being loaded in anticipation of a future need for that value.

The speculatively loaded value may or may not actually be used. It may be desirable to defer performing error correction for errors generated by speculative loads. The load instruction may be a special speculative load instruction that sets a testable flag to indicate that a speculative instruction is being executed that may be used as a speculative load indication. The software that issues the load instruction may know that the load is speculative and provide a speculative load indication.

A memory handler according to the present invention may receive a speculative load indication 106 that is true if the memory load request was issued speculatively. If the speculative load indication is not true 108, control is passed to the instructions for performing error recovery 120. If the memory fault indication is true 102 and the speculative load indication is true 108, then an error indication that the returned value is invalid may be provided 116. This allows error recovery to be deferred for errors that are detected during speculative memory accesses. Deferral is the process of generating a deferred exception indicator 116 and not performing the error recovery 120 at the time of its detection (and potentially never at all). The memory error handler returns 118 control to the program that invoked the memory error handler after providing the error indication 116. Deferring recovery of errors detected during speculative loads may avoid termination of an executing program for unrecoverable errors when the speculatively loaded value is not actually required by the executing program. Deferring recovery of correctable error may improve performance by avoiding the time required to perform error recovery of unused values. It may be possible for programs to use a speculative load for testing a memory location or a device for errors prior to using the memory location or device.

In the machine 10 shown in Figure 1, flag bits 14 are associated with the registers 12. The error indication may be returned by setting a value, such as false, into the flag bit 14 associated with the register 12 that is loaded with the returned value. The program that intends to use the loaded value may check the associated flag bit 14 to determine if the value is valid. If the value is invalid, the program may issue a non-speculative load for the value to force the memory error handling routine to perform error recovery. This may terminate

the executing program or this may provide a corrected value to the executing program.

The error indication may be returned by setting the returned value to an invalid value. For example, if the value is an integer with a sign bit, the value of negative zero could be defined as an invalid value that could be used to provide the error indication from the memory error handler. The program that intends to use the loaded value may check the value for validity before using the value. If the value is invalid, the program may issue a non-speculative load for the value to force the memory error handling routine to perform error recovery. This may terminate the executing program or this may provide a corrected value to the executing program.

In an embodiment of the invention on a machine that does not provide a mechanism for error recovery, the executing program may terminate if an invalid is detected with issuing a non-speculative load for the value.

Error recovery is performed 120 immediately if the memory fault indication is true 102 and the speculative load indication is not true 108. The memory error handler returns 122 control to the program that invoked the memory error handler after performing error recovery 122.

In another embodiment of the invention, the memory error handler may receive a fault deferral indication 110 that is true if faults can be deferred. This allows the treatment of errors on speculative loads by the memory error handler to be controlled. Another program, such as the executing program or the operating system, may set or clear the fault deferral indication to allow or prevent deferred recovery from errors on speculative loads. If the fault deferral indication is not true 112 error recovery 120 for errors generated by speculative loads is performed immediately. In other embodiments, the fault deferral indication may provide multiple states. This may allow non-recoverable errors to be deferred and cause correctable errors to be immediately corrected 114.

It will be appreciated that the invention is applicable to a variety of machines that load values from a memory. One example would be a central processor unit (CPU) loading values from a cache memory or a random access memory (RAM) or a secondary memory, such as a disk drive. Another

example would be a peripheral processor that loads values from a peripheral device, such as a network.

The Intel® IA-64 Architecture is an example of a processor architecture that supports speculative memory loads. The use of the invention with the IA-64 Architecture will be described as an exemplary embodiment of the invention. General registers 12 in the IA-64 provide a Not a Thing (NaT) bit 14 to provide a deferred exception indicator. Floating point registers provide a Not a Thing Value (NaTVal) to provide a deferred exception indicator. The present invention can use the NaT bit or the NaTVal as the error indication that the returned value is invalid. Once a deferred exception indicator is generated, it will propagate through all uses until the speculation is checked by using either a speculation check instruction or a non-speculative use. This causes the appropriate action to be invoked to deal with the exception.

Three different programming models are supported by the IA-64 Architecture: no-recovery, recovery and always-defer. These programming models are selected by bits in the Processor Status Register (PSR). In the no-recovery model, only fatal exceptional conditions are deferred--these are conditions which cannot be resolved without either involving the program's exception-handling code or terminating the program. The inventive memory handler will defer only uncorrectable memory errors. In the recovery model, performance may be increased by deferring additional exceptional conditions. The recovery model is used only if the program provides additional "recovery" code to re-execute failed speculative computations. In always-defer model, all exceptional conditions which can be deferred are deferred. This permits speculation in environments where faulting would be unrecoverable. The inventive memory handler will defer both correctable and uncorrectable memory errors in the recovery model and the always-defer model.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

CLAIMS

What is claimed is:

1. A method of handling memory errors comprising:
receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory;
receiving a speculative load indication that is true if the memory load request was issued speculatively; and
if the memory fault indication is true and the speculative load indication is true,
providing an error indication that the returned value is invalid,
otherwise,
performing error recovery.

2. The method of claim 1, wherein the error indication is a flag bit associated with the returned value.

3. The method of claim 1, wherein the error indication is setting the returned value to an invalid value.

4. The method of claim 1, further comprising receiving a fault deferral indication that is true if faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the fault deferral indication is true.

5. The method of claim 1, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.

6. A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory;

receiving a speculative load indication that is true if the memory load request was issued speculatively; and

if the memory fault indication is true and the speculative load indication is true,

providing an error indication that the returned value is invalid,

otherwise,

performing error recovery.

7. The machine-readable medium of claim 6, wherein the error indication is a flag bit associated with the returned value.

8. The machine-readable medium of claim 6, wherein the error indication is setting the returned value to an invalid value.

9. The machine-readable medium of claim 6, further comprising receiving a fault deferral indication that is true if faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the fault deferral indication is true.

10. The machine-readable medium of claim 6, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.

11. A machine comprising:
an interface to receive a value from a memory coupled to the machine;
a memory fault indicator that is true if an error in the memory is detected
while executing a memory load request to retrieve a value from the memory;
a speculative load indicator that is true if the memory load request was issued speculatively; and
a machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations including
if the memory fault indicator is true and the speculative load indicator is true,
providing an error indication that the returned value is invalid,
otherwise,
performing error recovery.

12. The machine of claim 11, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

13. The machine of claim 11, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

14. The machine of claim 11, further comprising receiving a fault deferral indicator from the machine to indicate that faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault indicator being true and the speculative load indicator being true, the fault deferral indicator is true.

15. The machine of claim 11, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.

16. A system comprising:
a machine;
a memory coupled to the machine; and
a machine-readable medium that provides instructions, which when executed by the machine, cause the machine to perform operations including
receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory,
receiving a speculative load indication that is true if the memory load request was issued speculatively, and
if the memory fault indication is true and the speculative load indication is true,
providing an error indication that the returned value is invalid,
otherwise,
performing error recovery.

17. The system of claim 16, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

18. The system of claim 16, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

19. The system of claim 16, further comprising receiving a fault deferral indicator from the machine to indicate that faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault

indicator being true and the speculative load indicator being true, the fault deferral indicator is true.

20. The system of claim 16, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.

ABSTRACT

A method of handling memory errors. A memory fault indication is received that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory. A speculative load indication is received that is true if the memory load request was issued speculatively. If the memory fault indication is true and the speculative load indication is true, then an error indication that the returned value is invalid is provided, otherwise, error recovery is performed.

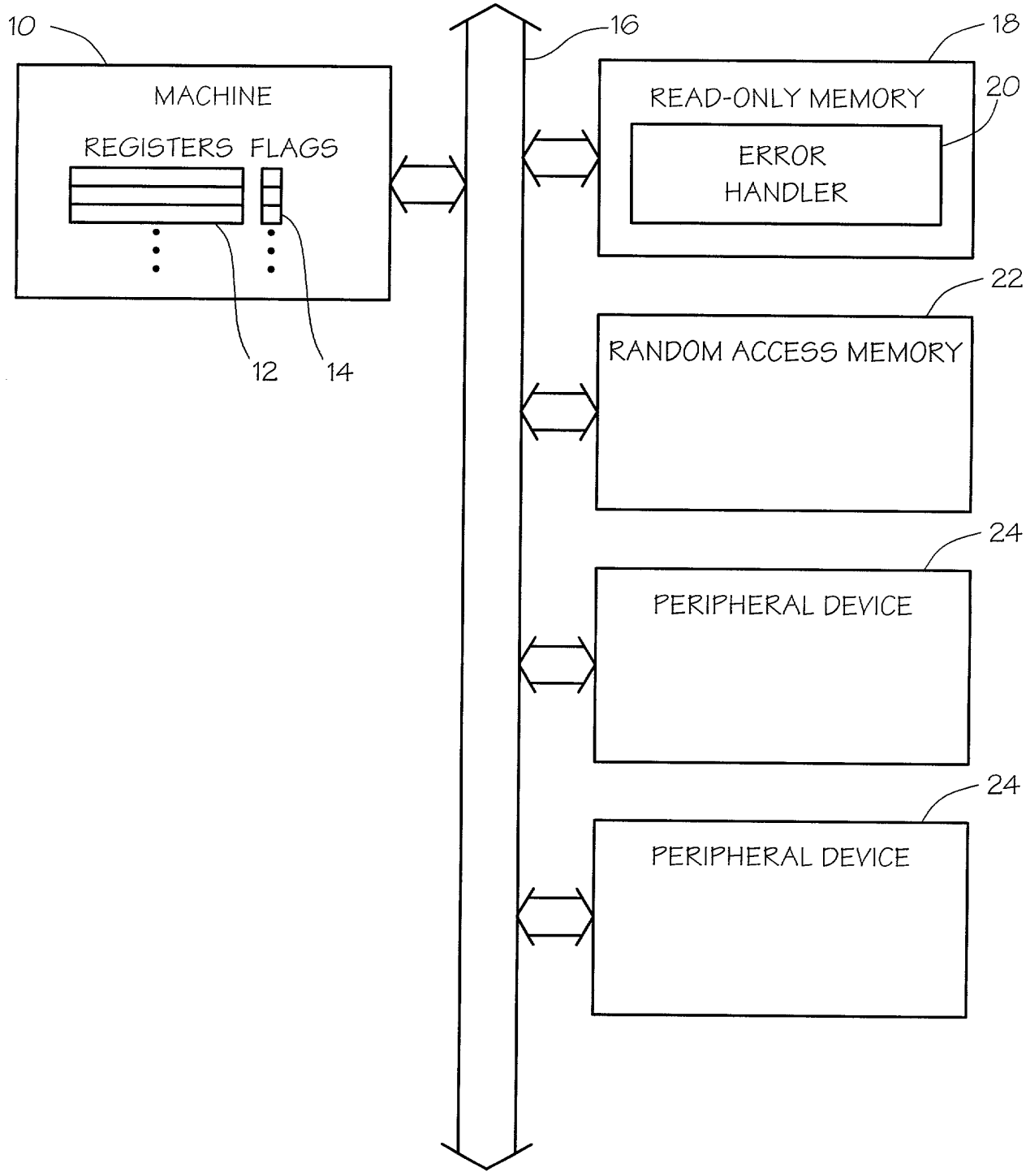
10
MACHINE
REGISTERS
FLAGS
12
14
16
18
READ-ONLY MEMORY
20
ERROR HANDLER
22
RANDOM ACCESS MEMORY
24
PERIPHERAL DEVICE
24
PERIPHERAL DEVICE

FIG. 1

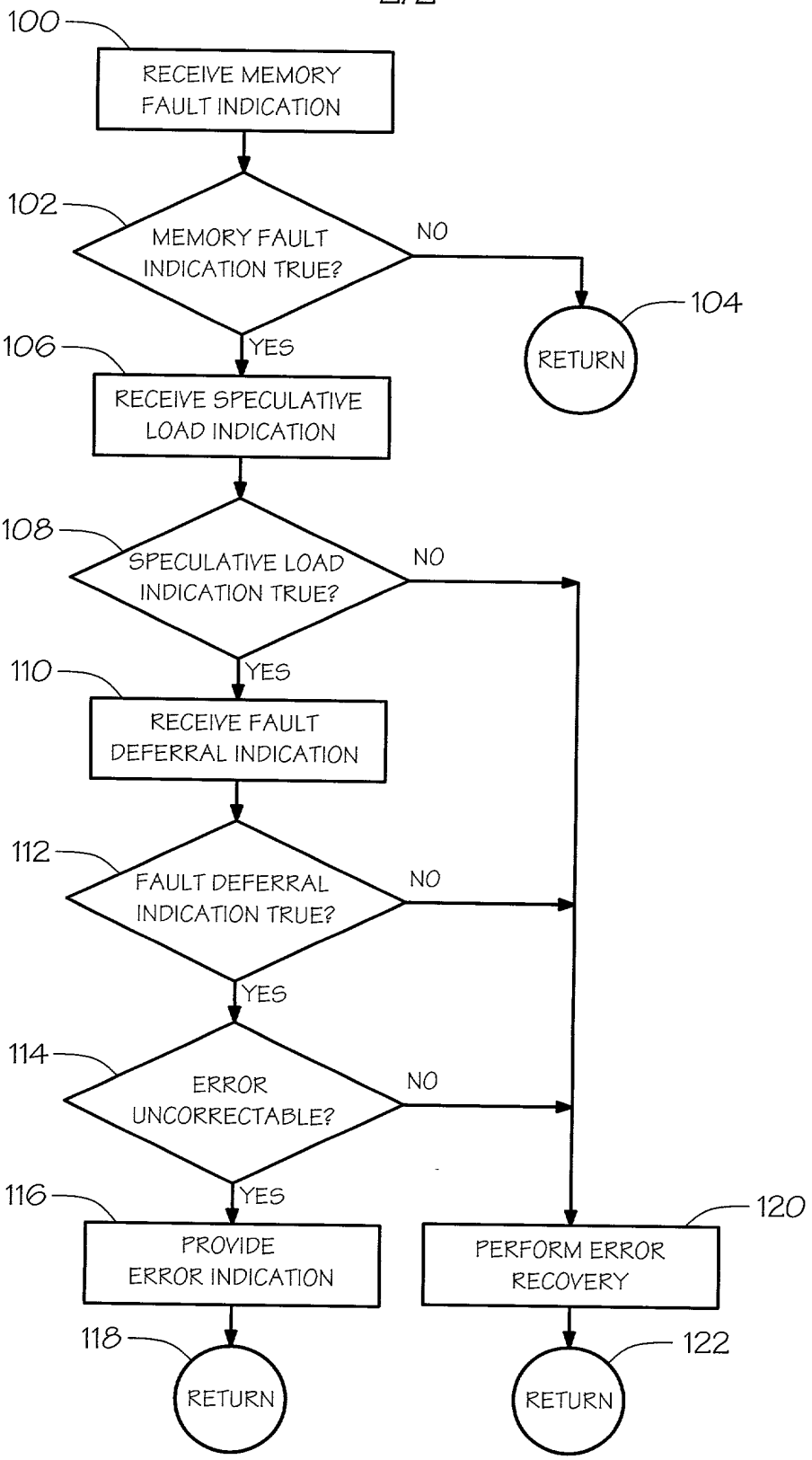
100
RECEIVE MEMORY FAULT INDICATION
102
MEMORY FAULT INDICATION TRUE?
NO
104
RETURN
YES
106
RECEIVE SPECULATIVE LOAD INDICATION
108
SPECULATIVE LOAD INDICATION TRUE?
NO
YES
110
RECEIVE FAULT DEFERRAL INDICATION
112
FAULT DEFERRAL INDICATION TRUE?
NO
YES
114
ERROR UNCORRECTABLE?
NO
YES
116
PROVIDE ERROR INDICATION
120
PERFORM ERROR RECOVERY
118
RETURN
122
RETURN

FIG. 2

Attorney's Docket No.: 042390.P5727

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ERROR RECOVERY FOR SPECULATIVE MEMORY ACCESSES

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to:
James Henry, Reg. No. 41,064, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
(Name of Attorney or Agent)
12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to:
James Henry, (714) 557-3800.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature _____ Date _____

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Full Name of Fourth/Joint Inventor (given name, family name) _____

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Full Name of Fifth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ (City , State) Citizenship _____ (Country)

P. O. Address _____

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Full Name of Sixth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

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(City , State) *(Country)*

P. O. Address _____

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Full Name of Seventh/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

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(City , State) *(Country)*

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Full Name of Eighth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

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Full Name of Ninth/Joint Inventor (given name, family name) _____

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Full Name of Tenth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

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Full Name of Eleventh/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
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_____

APPENDIX A

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Lisa N. Benado, Reg. No. 39,995; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Gregory D. Caldwell, Reg. No. 39,926; Andrew C. Chen, Reg. No. 43,544; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Dennis M. deGuzman, Reg. No. 41,702; Stephen M. De Klerk, Reg. No. P46,503; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Sanjeet Dutta, Reg. No. P46,145; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; George Fountain, Reg. No. 36,374; Paramita Ghosh, Reg. No. 42,806; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Sang Hui Kim, Reg. No. 40,450; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Erica W. Kuo, Reg. No. 42,775; George B. Leavell, Reg. No. 45,436; Gordon R. Lindeen III, Reg. No. 33,192; Jan Carol Little, Reg. No. 41,181; Kurt P. Leyendecker, Reg. No. 42,799; Joseph Lutz, Reg. No. 43,765; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Daniel E. Ovanezian, Reg. No. 41,236; Kenneth B. Paley, Reg. No. 38,989; Marina Portnova, Reg. No. P45,750; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; Joseph A. Twarowski, Reg. No. 42,191; Thomas A. Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. P46,322; Thomas C. Webster, Reg. No. P46,154; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Firasat Ali, Reg. No. 45,715; and Justin M. Dillon, Reg. No. 42,486; Raul Martinez, Reg. No. 46,904; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (714) 557-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; John N. Greaves, Reg. No. 40,362; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. 44,855; Gene I. Su, Reg. No. 45,140; and Steven D. Yates, Reg. No. 42,242, my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.